REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, applicant has cancelled claims 9 and 10, amended claims 1 and 18-19, and added new claims 20-23. Claims 1-8 and 17-23 are currently pending.

In the Office Action mailed February 7, 2003, the Examiner rejected the pending claims as unpatentable over the prior art. To the extent that these rejections might still be applied to the claims as amended, they are respectfully traversed as follows.

In Paragraph 2 of the Office Action, the Examiner contends that the first solder material 10 of Froloff et al may be lead-based solder while the second solder material 9 may be tin-based alloy. However, such disclosure is not given in Froloff et al. Column 3, lines 37-59 of Froloff et al merely sets forth that the soft solder layers 9 and 10 are formed of one of tin solders, cadmium solders, zinc solders and lead solders, but no more and no less. Froloff et al never teaches or suggests that the soft solder layers 9, 10 are made of different solder materials, let alone the claimed time-differential solidification of the first and second solder materials. Thus, the Examiner's interpretation of Froloff is plainly erroneous.

Notwithstanding the Examiner's erroneous holding, applicant has amended the claims while adding new claims 20-22. Claims 18 and 19 have been amended with respect to their dependency. Claims 9 and 10 have been replaced with new claims 20 and 21 which depend from claims 18 and 19, respectively. New claim 22 is an independent claim that corresponds to former claim 3 held allowable by the Examiner and which therefore should be allowable. New

claim 23 is an independent claim that corresponds to former claim 4 held allowable by the Examiner and which therefore should be allowable.

Amended claim 1 now sets forth, among other things, that the lower conductor includes a die pad portion for mounting the semiconductor chip, and that the first solder material is caused to solidify earlier than the second solder material in the solidifying step for securing the semiconductor chip on the die pad portion of the lower conductor before the upper conductor is fixedly connected to the semiconductor chip. The underlined feature reflects the core of the present invention which aims to prevent improper mounting of the semiconductor chip when the first solder material and the second solder material are solidified simultaneously, as shown in Fig. 20.

As previously pointed out, Froloff et al merely teaches different candidate solder materials but fails to suggest using one solder material for one solder layer 9 and a different solder material for the other solder layer 10. According to Froloff et al, soldering is performed in a simple process, which per se is known for the use of soft solder (column 4, line 24-27). Note that the claimed time-differential solidification of the present invention is not known.

Applicant respectfully submits that the Examiner's reasoning for his rejection is plainly mistaken. Should the Examiner maintain this position, applicant requests the courtesy of a phone call to schedule a personal interview with the Examiner and his supervisor, Mr. Tom Thomas.

In view of the foregoing all of the claims in this case are believed to be in condition for allowance. Should the Examiner have any questions or determine that any further action is

desirable to place this application in even better condition for issue, the Examiner is encouraged to telephone applicants' undersigned representative at the number listed below.

Respectfully submitted,

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Date: May 7, 2003

Attachments: Amended Claims w/ Markings

MDB/lrhj

Customer No. 28970

VERSION WITH MARKINGS TO SHOW CHANGES MADE TO CLAIMS

1. (Twice Amended) A method of making a semiconductor device, the method comprising the steps of:

mounting a semiconductor chip on a lower conductor, with first solder material applied between the chip and the lower conductor;

positioning an upper conductor on the chip, with second solder material applied between the chip and the upper conductor;

heating up the first and the second solder materials beyond melting points of the respective materials; and

solidifying the first and the second solder materials;

wherein the lower conductor includes a die pad portion for mounting the semiconductor chip; and

wherein the first solder material is caused to solidify earlier than the second solder material in the solidifying step for securing the semiconductor chip on the die pad portion of the lower conductor before the upper conductor is fixedly connected to the semiconductor chip.

9. Deleted

10. Deleted

18. (Amended) The method according to claim [12] 17, wherein the lower conductor further comprises [a die pad portion and] lower lead portions extending from the die pad portion. [on which the semiconductor chip is to be mounted.]

19. (Amended) The method according to claim [13] 18, wherein the second conductive pattern comprises upper lead portions at least one of which is to be connected to the semiconductor chip as the upper conductor.

20. (New) The method according to claim 19, further comprising the step of removing at least one of the lower and the upper lead portions from the frame.

21. (New) The method according to clam 19, wherein the frame comprises first and second common bars parallel to each other, the upper lead portions being divided into first and second groups, the upper lead portions in the first group extending from the first common bar toward the second common bar, the upper lead portions in the second group extending from the second common bar toward the first common bar.

22. (New) A method of making a semiconductor device, the method comprising the steps of:

mounting a semiconductor chip on a lower conductor, with first solder material applied between the chip and the lower conductor;

positioning an upper conductor on the chip, with second solder material applied between the chip and the upper conductor;

heating up the first and the second solder materials beyond melting points of the respective materials; and

solidifying the first and the second solder materials;

wherein the first solder material is caused to solidify earlier than the second solder material in the solidifying step; and

wherein the heating of the first solder material is terminated earlier than the heating of the second solder material.

23. (New) A method of making a semiconductor device, the method comprising the steps of:

mounting a semiconductor chip on a lower conductor, with first solder material applied between the chip and the lower conductor;

positioning an upper conductor on the chip, with second solder material applied between the chip and the upper conductor;

heating up the first and the second solder materials beyond melting points of the respective materials; and

solidifying the first and the second solder materials;

wherein the first solder material is caused to solidify earlier than the second solder material in the solidifying step; and

wherein the heating of the first and the second solder materials is performed by contacting the lower and the upper conductors with first and second heaters, respectively.